

IPC100N04S5-1R2-VB Datasheet

N-Channel 40V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.00086
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.00116
Q_g typ. (nC)	59.2
I_D (A) ^{a, g}	180
Configuration	Single

FEATURES

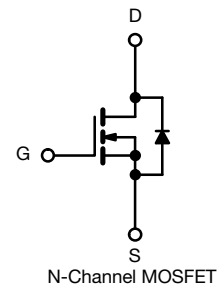
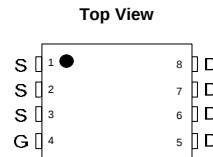
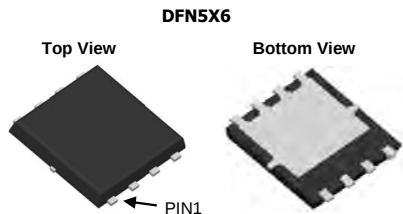
- Trench Gen IV power MOSFET
- 100 % R_g and UIS tested
- Q_{gd}/Q_{gs} ratio < 1 optimizes switching characteristics

APPLICATIONS

- Synchronous rectification
- OR-ing
- High power density DC/DC
- VRMs and embedded DC/DC
- DC/AC inverters
- Load switch



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	+20, -16	
Continuous drain current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	180 ^g
		$T_C = 70^\circ\text{C}$	144 ^g
		$T_A = 25^\circ\text{C}$	72 ^{b, c}
		$T_A = 70^\circ\text{C}$	36 ^{b, c}
Pulsed drain current ($t = 100 \mu\text{s}$)	I_{DM}	720	A
Continuous source-drain diode current	I_S	$T_C = 25^\circ\text{C}$	90
		$T_A = 25^\circ\text{C}$	5.6 ^{b, c}
Single pulse avalanche current	I_{AS}	45	
Single pulse avalanche Energy	E_{AS}	101	mJ
Maximum power dissipation	P_D	$T_C = 25^\circ\text{C}$	100
		$T_C = 70^\circ\text{C}$	64
		$T_A = 25^\circ\text{C}$	6.25 ^{b, c}
		$T_A = 70^\circ\text{C}$	4 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, f}	R_{thJA}	15	20	$^\circ\text{C}/\text{W}$
Maximum junction-to-case (drain)	R_{thJC}	0.95	1.25	

Notes

- Based on $T_C = 25^\circ\text{C}$
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- The DFN5x6 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is $54^\circ\text{C}/\text{W}$
- Package limited

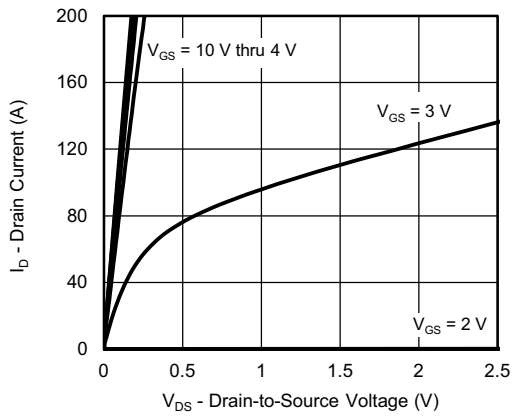
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	25	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	-5.6	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2.2	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.00086	-	Ω
		V _{GS} = 4.5 V, I _D = 15 A	-	0.00116	-	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 20 A	-	106	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	8445	-	pF
Output capacitance	C _{oss}		-	1310	-	
Reverse transfer capacitance	C _{rss}		-	110	-	
C _{rss} /C _{iss} ratio				-	0.013	0.026
Total gate charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 60 A	-	129	194	nC
		V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 60 A	-	59.2	89	
Gate-source charge	Q _{gs}		-	25	-	
Gate-drain charge	Q _{gd}		-	13	-	
Output charge	Q _{oss}	V _{DS} = 20 V, V _{GS} = 0 V	-	61	-	
Gate resistance	R _g	f = 1 MHz	0.2	0.7	1.2	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 1 Ω I _D ≅ 60 A, V _{GEN} = 10 V, R _g = 1 Ω	-	19	38	ns
Rise time	t _r		-	10	20	
Turn-off delay time	t _{d(off)}		-	53	106	
Fall time	t _f		-	10	20	
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 1 Ω I _D ≅ 60 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	56	112	
Rise time	t _r		-	159	318	
Turn-off delay time	t _{d(off)}		-	54	108	
Fall time	t _f		-	36	72	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	180	A
Pulse diode forward current (t _p = 100 μs)	I _{SM}		-	-	720	
Body diode voltage	V _{SD}	I _S = 30 A	-	0.71	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 30 A, di/dt = 100 A/μs, T _J = 25 °C	-	64	128	ns
Body diode reverse recovery charge	Q _{rr}		-	116	232	nC
Reverse recovery fall time	t _a		-	40	-	ns
Reverse recovery rise time	t _b		-	24	-	

Notes

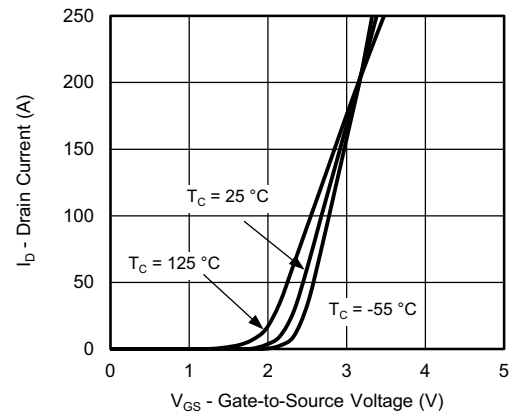
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
 b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

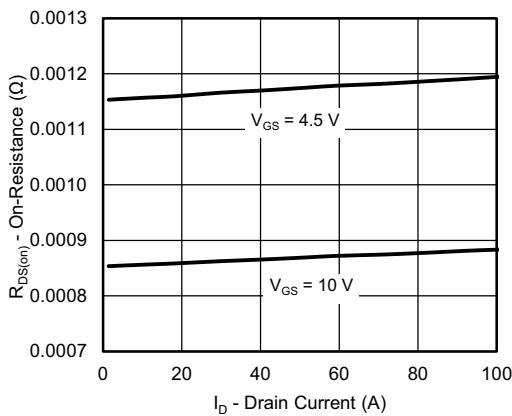
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



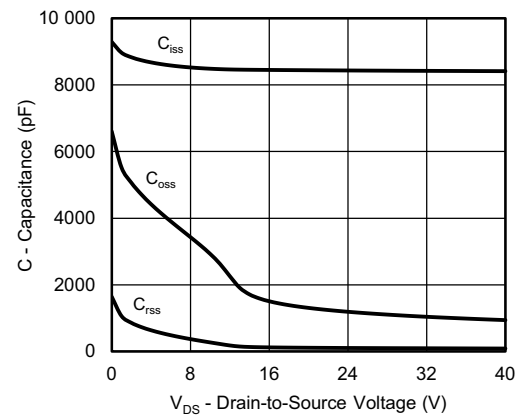
Output Characteristics



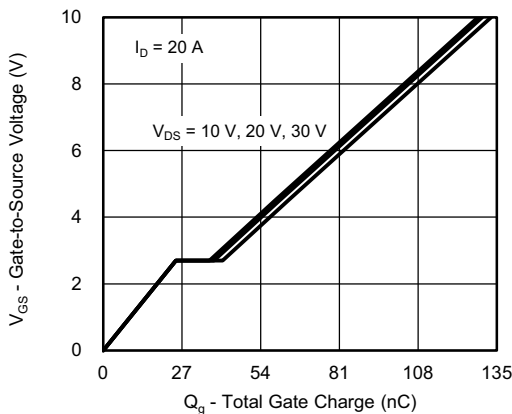
Transfer Characteristics



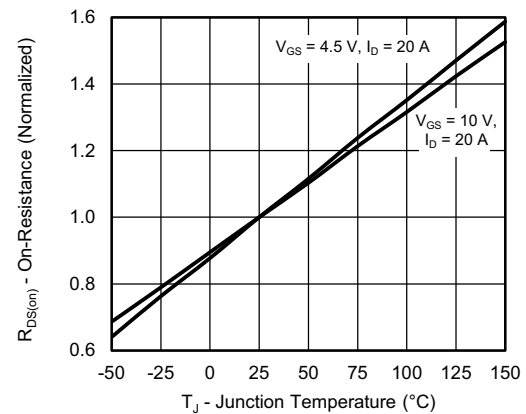
On-Resistance vs. Drain Current



Capacitance

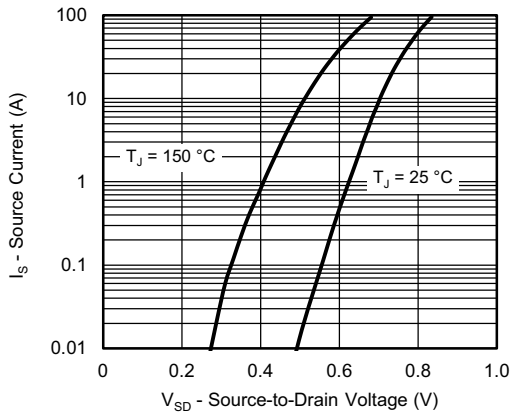


Gate Charge

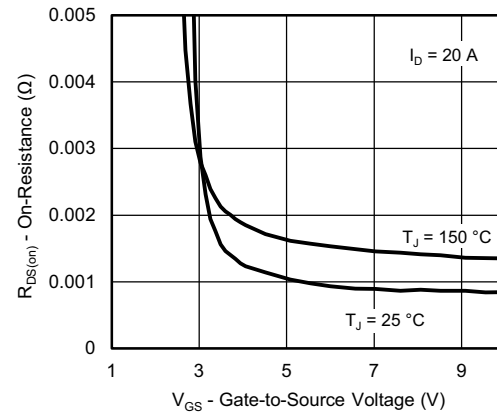


On-Resistance vs. Junction Temperature

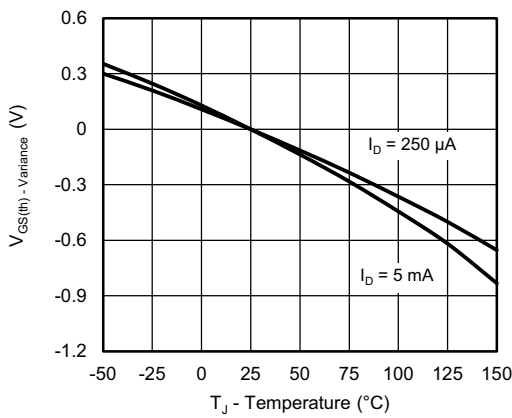
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



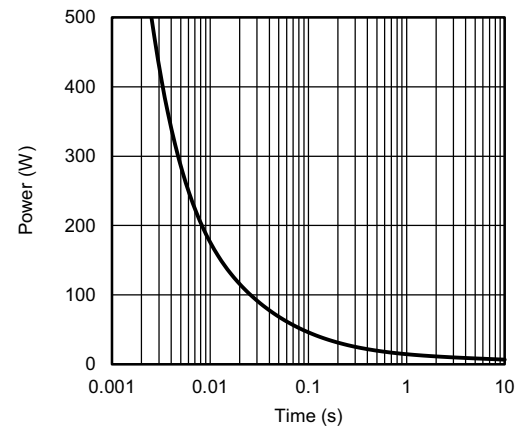
Source-Drain Diode Forward Voltage



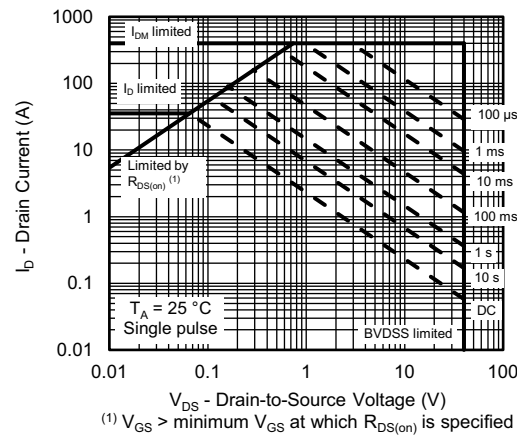
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



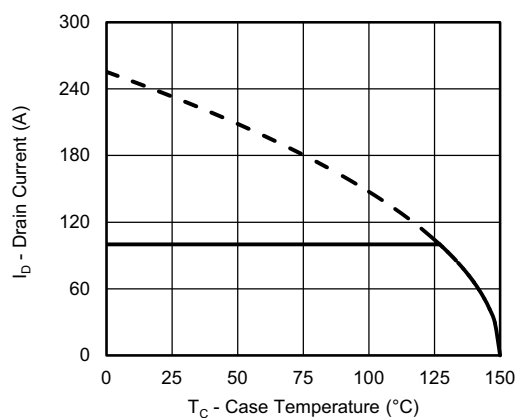
Single Pulse Power, Junction-to-Ambient



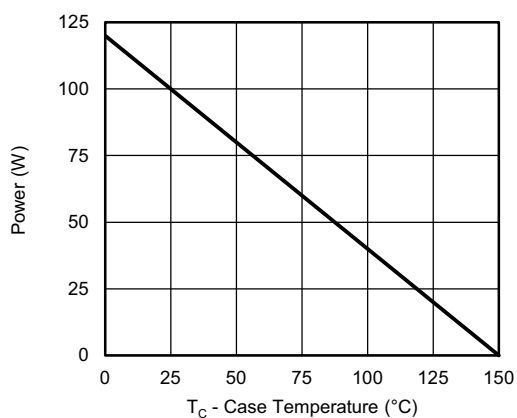
Safe Operating Area

(1) $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

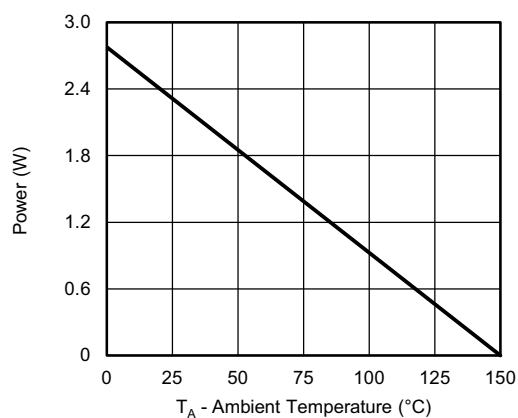
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case

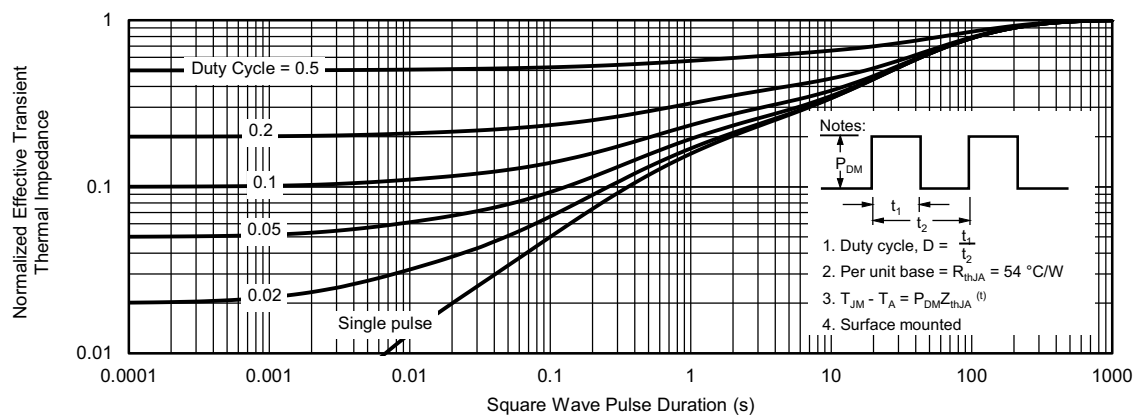


Power, Junction-to-Ambient

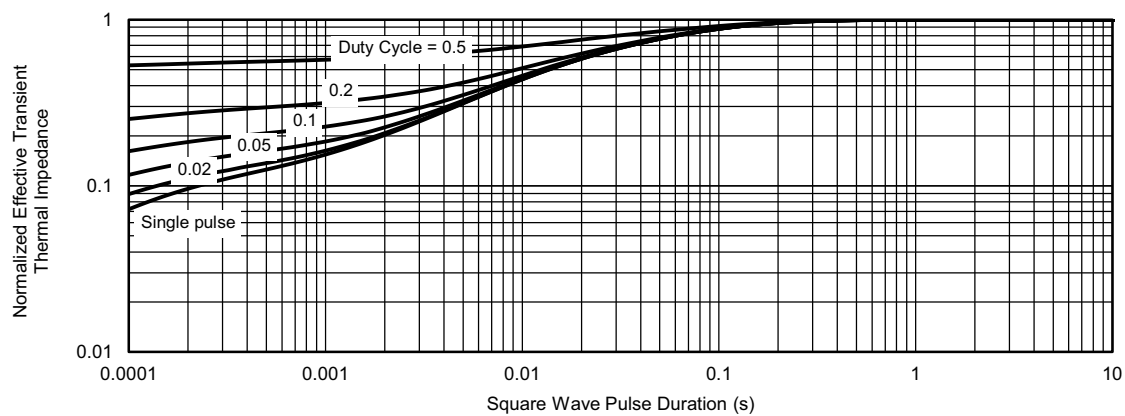
Note

- a. The power dissipation P_D is based on $T_J \text{ max.} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

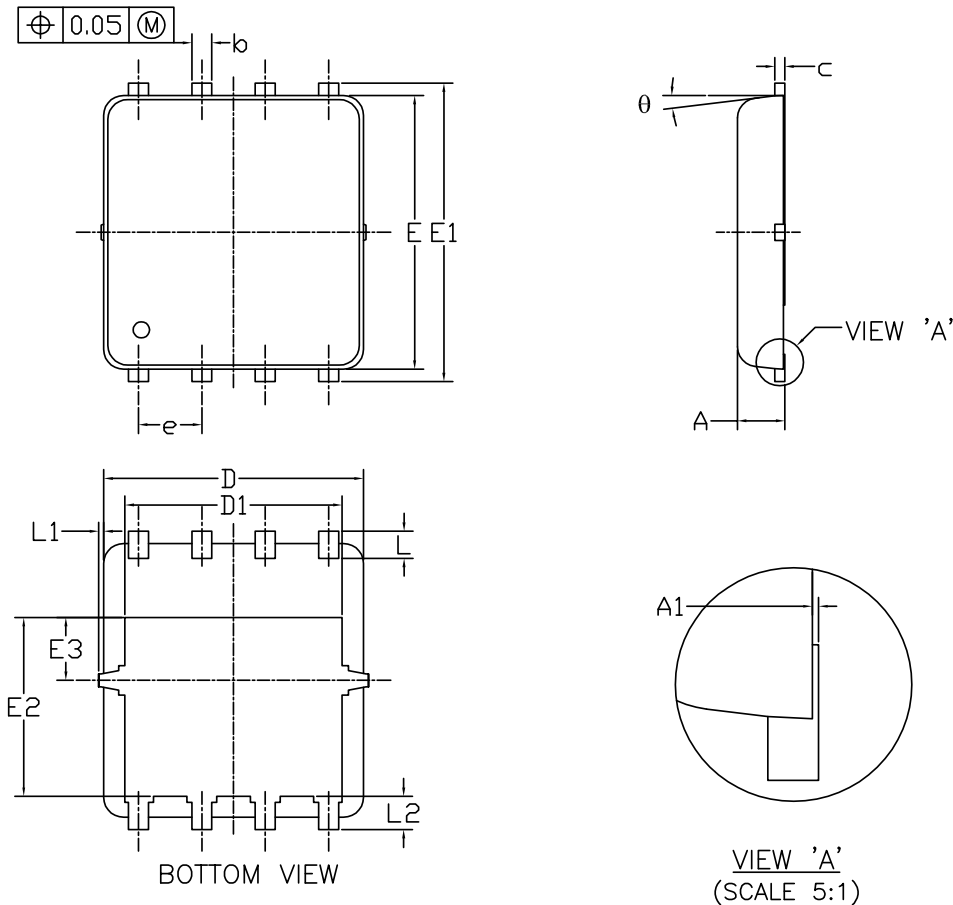


Normalized Thermal Transient Impedance, Junction-to-Ambient

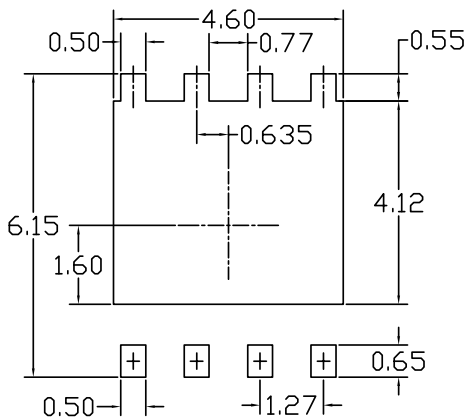


Normalized Thermal Transient Impedance, Junction-to-Case

DFN5x6_8L_EP1_P PACKAGE OUTLIN



RECOMMENDED LAND PATTERN



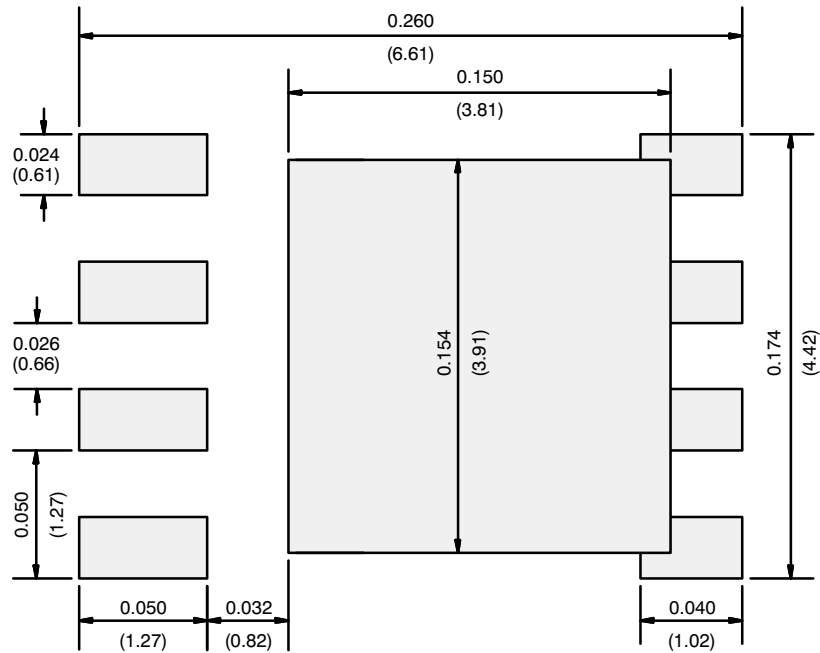
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	---	0.05	0.000	---	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.10	5.20	5.30	0.201	0.205	0.209
D1	4.25	4.35	4.45	0.167	0.171	0.175
E	5.45	5.55	5.65	0.215	0.219	0.222
E1	5.95	6.05	6.15	0.234	0.238	0.242
E2	3.525	3.625	3.725	0.139	0.143	0.147
E3	1.175	1.275	1.375	0.046	0.050	0.054
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	---	0.15	0	---	0.006
L2	0.68 REF			0.027 REF		
theta	0°	---	10°	0°	---	10°

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

UNIT: mm

RECOMMENDED MINIMUM PADS



Dimensions in Inches/(mm)

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